REMARKS

Reconsideration and allowance are requested.

Claims 19-27 stand rejected under 35 U.S.C. §101 with the Examiner requiring that the computer program be embodied in a computer-readable medium. Claim 19 has been so amended. Withdrawal of this rejection is requested.

Applicants note with appreciation the indication of allowable subject matter in claims 5, 14, and 23. New claims 28-48 have been added. Independent claims 28, 35, and 42 are based on the allowable subject matter of claims 5, 14, and 23. Accordingly, claims 28-48 should be allowed.

Claims 1-4, 6-13, 15-22, and 24-27 stand rejected under 35 U.S.C. §102 for anticipation based on Mahon's The Hewlett-Packard Precision Architecture (HP-PA). This rejection is respectfully traversed.

The originally-filed independent claims 1, 10, and 19 have been amended to specify that the offset value is an unsigned value, and that only the form of instruction with the smaller maximum offset value size supports the manipulation of either adding or subtracting the unsigned offset value. For example, claim 1 now recites:

> said offset value is an unsigned value; and
>
> a manipulation supported by said second form but not by said first form forms a modified address value by a specifiable one of:
>
> adding said offset value to said base address value; and
>
> subtracting said offset value from said base address value.

Example support for these amendments may be found on page 9 of the application which describes the offset value as being zero-extended, and such zero-extension is only applicable to

unsigned values. As explained at lines 30-31 on page 9, the U-bit in the second form of instruction specifies whether the zero-extended offset value is to be added to or subtracted from the base address value to form a modified address value. This option is not provided for the first form of instruction described in relation to Figure 2.

Mahon only allows for symmetric offset ranges: offsets from -8192 to +8191 for "Load Word" and from -16 to +15 "Load Word Short." In contrast, independent claims 1, 10, and 19 also provide an asymmetric range of possible offsets for the "longer offset with fewer manipulations" first form of instruction. Consider the non-limiting example embodiment described in the application. The first form of instruction gives asymmetric offsets from 0 to +4095, while the second form of instruction gives symmetric offsets from -255 to +255. This feature is advantageous because large positive offsets are in practice much more frequent than large negative offsets (the reason being that pointers to large data structures point to the lowest address within them by common practice). Thus, supporting only large positive offsets in the first form of instruction makes more efficient use of the instruction bit space. As a result, the instruction bit space that is released by not supporting large negative offsets is thus available for other useful purposes.

The anticipation rejection having been overcome, the application is in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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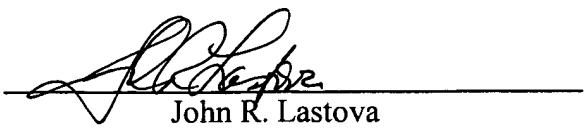
By: 
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